05-24-00

A

jc820 U.S. PTO 05/23/00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: BALLINGER
Docket: 30019.100USU1
Title: PSEUDO–NOISE ENCODED DIGITAL DATA CLOCK RECOVERY

jc658 U.S. PTO 09/576056 05/23/00

CERTIFICATE UNDER 37 CFR 1 10
'Express Mail' mailing label number: EL544514405US
Date of Deposit: May 23, 2000
I hereby certify that this paper or fee is being deposited with the United States Postal Service 'Express Mail Post Office To Addressee' service under 37 CFR 1.10 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

By: Linda McCormick
Name: Linda McCormick

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

We are transmitting herewith the attached:

- ☒ Transmittal sheet, in duplicate, containing Certificate under 37 CFR 1.10.
- ☒ Utility Patent Application: Spec. 28 pgs; 56 claims; Abstract 1 pgs. The fee has been calculated as shown below in the 'Claims as Filed' table.
- ☒ 9 sheets of informal drawings
- ☒ A signed Combined Declaration and Power of Attorney
- ☒ Assignment of the invention to Level One Communications, Inc., Recordation Form Cover Sheet
- ☒ A check in the amount of $1494.00 to cover the Filing Fee
- ☒ A check for $40.00 to cover the Assignment Recording Fee.
- ☒ Return postcard

CLAIMS AS FILED

Number of Claims Filed		In Excess of:		Number Extra		Rate		Fee
Basic Filing Fee								$690.00
Total Claims								
56	–	20	=	36	x	18.00	=	$648.00
Independent Claims								
5	–	3	=	2	x	78.00	=	$156.00
MULTIPLE DEPENDENT CLAIM FEE								$0.00
TOTAL FILING FEE								$1494.00

Please charge any additional fees or credit overpayment to Deposit Account No. 13–2725. A duplicate of this sheet is enclosed.

MERCHANT & GOULD P.C.
P.O. Box 2903, Minneapolis, MN 55402–0903
(612) 332–5300

By: Min S. Xu
Name: Min S. Xu
Reg. No.: 39,536
Initials: AX:PSTkls

(PTO TRANSMITTAL – NEW FILING)

PSEUDO-NOISE ENCODED DIGITAL DATA CLOCK RECOVERY

RELATED APPLICATION

This application claims the benefit of Provisional Application, U.S. Serial No. 60/135,571, filed on May 24, 1999, entitled "PSEUDO-NOISE ENCODED DIGITAL DATA CLOCK RECOVERY", by David Ballinger.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates in general to a communication system, and more particularly to a pseudo-noise encoded digital data clock recovery circuit at a receiver of a communication system.

2. Description of Related Art

In communication systems, signals or data are modulated at a transmission end before they are transmitted to a transmission media. At a receiving end, the signals are recovered/demodulated/acquired. Due to the noise and other defects in the transmission media, the received signals often carry errors, such as noise signals, phase shifts, etc. To overcome these problems, communication systems often use an error correcting technique in a recovery circuit at the receiving end to reliably recover the original signals or data. One technique is to use a pseudo-noise encoded digital data clock recovery

circuit by correlating a pseudo-noise sequence which is used to encode/modulate the original signals or data at the transmission end with the received signals. More specifically, a serial stream of digital signals or data is modulated by a pseudo-noise sequence known to both a transmitter and a receiver of a communication system. The pseudo-noise sequence is a finite length pseudo-random sequence of bits (e.g., 101100111101000). In this type of modulation, "1" bits in the original data stream are replaced by the true pseudo-noise sequence (e.g., 101100111101000) and "0" bits are replaced by the complement of the true pseudo-noise sequence (e.g. 010011000010111), respectively. Thus, the bit rate of the modulated data stream is M times the bit rate of the original data stream where M is the number of bits in the pseudo-noise sequence, e.g. M is fifteen (15).

Traditionally, the individual bits in a pseudo-noise sequence are often referred to as "chips". Henceforth, the bits in the original data stream is hereinafter referred to as "bits", and the pseudo-noise bits in the modulated data stream is hereinafter referred to as "chips".

In the existing communication systems, an additional modulation step is usually used, whereby an analog carrier signal is modulated by the pseudo-noise modulated data stream for effective transmission over a physical medium (e.g., PSK, FM). In some systems, a received signal is first demodulated to recover the pseudo-noise modulated chip stream generated by at the transmitter, while other systems recover an original bit stream directly from the received analog signal in one demodulation step.

Typically, the receiver can recover the original bit stream by looking for matches of the pseudo-noise sequence or its complement, within the incoming chip stream. However, if the transmission media is noisy resulting in frequent chip errors, a more sophisticated method is needed to recover the data. The greater the chip error rate, the more difficult it is to recognize the pseudo-noise sequence or its complement in a received chip stream. A bit period is defined as the time interval spanned by one bit before pseudo-noise modulation and by the M chips of the true or complement pseudo-noise sequence after modulation. If an alignment of the original bit period within the chip stream is known, then the data can be recovered by comparing the chips in the pseudo-noise sequence with their counterparts in the incoming chip stream and counting up the matches. If the number of matches is close to the number of chips in the pseudo-noise sequence, then the original bit is most likely a One (1 bit). Otherwise, if the number of matches is close to zero, then the original bit is most likely a Zero (0 bit). If the number of matches falls somewhere near the middle of the range, i.e. falls somewhere near the middle between zero and the number of chips in the pseudo-noise sequence, then most likely the presumed alignment of the original bit period is not correct. In fact, the alignment of the bit period within the received chip stream must be precisely identified before the original data can be reliably recovered.

In the existing communication systems, a correct bit period is typically identified by correlating the chip stream with the pseudo-noise sequence. Specifically, a chip stream is shifted through a correlator circuit that, at each shift increment, attempts to

match the sequence of chips in the correlator with the pseudo-noise sequence and outputs the number of matching chips. Once a pseudo-noise sequence alignment is found, then the correlator can be used to recover the original data stream. Typically, if the pseudo-noise sequence is chosen carefully, even with a high chip error rate, the correlator will produce a value near one of the extremes of its range, i.e. zero to M, if a bit period of the chip stream is perfectly aligned with the correlator's reference pseudo-noise sequence and a value near the middle of its range otherwise.

In the existing communication systems, an upper and a lower threshold is applied to a correlator output. As a result, a thresholded correlator output is generated. The thresholded correlator output indicates whether the correlator has exceeded either the upper or lower threshold. In other words, the thresholded correlator output indicates whether the correlator output is near one of the extremes and not in the middle. One would expect to see a spike (binary one) on a correlator output every time a true or its complement pseudo-noise sequence in the incoming chip stream comes into alignment with the correlator's reference pseudo-noise sequence. A binary signal, called a "bit clock" or "detection signal", is derived from the thresholded correlator output. The bit clock or detection signal is a periodic signal which indicates when the output of the correlator should be looked at to determine the original bit stream, i.e., when the bit period of the incoming chip stream is presumed to be aligned with the reference pseudo-noise sequence in the correlator.

The simplest derivation of the bit clock is to use a thresholded correlator output. If the chip error rate is low enough, then this scheme is sufficient to produce a reliable, periodic bit clock with no misaligned or dropped cycles. Ideally, the correlator output does not produce spurious spikes in between bit period boundaries or drops spikes at bit period boundaries. Alternatively, a clock divider, which is resynchronized to spikes of the correlator output when those spikes are deemed to mark true bit boundaries, could generate a bit clock. For example, a bit clock could be generated with a fairly high degree of confidence if the bit clock is resynchronized only after observing some number N consecutive spikes of the same periodicity as the bit rate on the correlator output.

Typically, clocks used at the transmitter and receiver of a communication system are not synchronized because their oscillators are independent. Therefore, the derived bit clock at the receiver often drifts out of phase with respect to a bit period in the transmitted signal unless its synchronization is maintained. The problem of identifying the correct bit period alignment covers not only an initial identification of this alignment ("acquisition") but also the maintaining of the correct alignment over time ("tracking"). In the existing systems, a correlator output is used to periodically adjust the phase of the bit clock in the same way that the correlator output is used to initially synchronize the bit clock.

Also, in some existing systems, the received chip stream is oversampled by a rate that is the chip rate multiplied by a whole number. The resulting stream is correlated with the pseudo-noise sequence in much the same way as before, except instead of

comparing every element in the correlator shift register with the pseudo-noise sequence, every Kth element is compared with the pseudo-noise sequence, where K is the number of samples per chip.

Oversampling techniques have advantages for bit clock phase alignment. In a system using an oversampling technique, a thresholded correlator output would produce a series of K consecutive spikes once every bit period. In theory, the data clock recovery circuit could use the correlator output at any of the sample positions associated with this series. However, with errors in the received chip stream or with phase drift between the transmitter and receiver clocks, the optimal sample position for data recovery is typically the one that occurs in the center of the intervals where this series of spikes is expected on the correlator output.

In receivers where there is one sample per chip, and there is phase drift between the transmitter and the receiver, bit clock tracking is problematic. When the optimal sample position of the correlator output drifts from one position to an adjacent position, the phase of the generated bit clock follows the drift with a small time lag since it takes at least one bit period for the bit clock to synchronize. With multiple samples per chip, the problem is solved. The bit clock phase can be off by one sample position from the optimal sample position but does not compromise the recovery of the data. In receivers where there is only one sample per chip, if the bit clock is off by one sample position, then the recovered data would be erroneous.

In systems where there are multiple samples per chip, chips are generally recovered in a lower error rate when the chips are sampled nearer to the center of the chip period. This results in a more reliable correlator output. Therefore, if the received chip stream is sampled multiple times in each chip period, then the bit clock generator can choose the best sample position within the interval of expected spikes at the thresholded correlator output.

However, in applications with particularly high chip error rates, e.g. 1 in 10 or 1 in 5, the oversampling technique and other techniques described above are not sufficiently robust to align the bit clock with a high degree of confidence. With such error rates, the correlator frequently generates false spikes on its threshold output when a pseudo-noise sequence is not aligned with the bit period of the incoming chip stream and, conversely, the correlator does not generate correct spikes even when a pseudo-noise sequence is aligned with the bit period of the incoming chip stream.

It can be seen then that there is a need for a pseudo-noise encoded digital data clock recovery circuit that reliably synchronizes a bit clock, identifies a correct bit alignment, and tracks the correct bit alignment over time.

It can also be seen that there is a need for a pseudo-noise encoded digital data clock recovery circuit that recovers an original bit stream from a digital chip stream in a noisy transmission media with high error rates.

It is with respect to these and other considerations that the present invention has been made.

SUMMARY OF THE INVENTION

To overcome the limitations in the prior art described above, and to overcome other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a pseudo-noise encoded digital data clock recovery circuit that recovers an original bit stream from a received chip stream.

The present invention solves the above-described problems by providing a pseudo-noise encoded digital data clock recovery circuit that reliably synchronizes a bit clock, identifies a correct bit alignment, and tracks a correct bit alignment over time.

In one embodiment in accordance with the principles of the present invention, a method for recovering an original bit stream from a received chip stream in a communication system includes the steps of maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and synchronizing a bit clock by using the history of correlation.

Still in one embodiment, the step of maintaining the history of correlation includes histogramming a correlator output over all possible sample positions for the bit clock. In another embodiment, the step of maintaining the history of correlation includes histogramming a correlator output over a finite window of sample positions for the bit clock.

Further in one embodiment, the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods. In another embodiment,

the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

In one embodiment, the method further includes the steps of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output. The step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter at the all possible sampling positions. In another embodiment, the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

Yet in one embodiment, the step of synchronizing the bit clock is based on the histogram of the counters or accumulators that exceed a preset threshold. In another embodiment, the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

The present invention also provides a pseudo-noise encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream. In one embodiment, the circuit includes: a correlator for correlating a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence modulating the original bit stream; a phase controller, coupled to the correlator, being configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods; and a bit clock generator, coupled to the phase controller, for generating a bit clock which determines a sampling position of the received chip stream

to recover the original bit stream from the received chip stream, the bit clock generator using the histogram of the correlator output to select/adjust the sample position for the bit clock.

These and various other advantages and features of novelty which characterize the invention are pointed out with particularity in the claims annexed hereto and form a part hereof. However, for a better understanding of the invention, its advantages, and the objects obtained by its use, reference should be made to the drawings which form a further part hereof, and to accompanying descriptive matter, in which there are illustrated and described specific examples of an apparatus in accordance with the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

Fig. 1 illustrates a diagram of an exemplary communication system using a pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention;

Fig. 2 illustrates a diagram of an exemplary original bit stream (a) at a transmitter, a corresponding pseudo-noise sequence encoded chip stream (b) at a transmitter, and a corresponding correlator output (c), over six bit periods;

Fig. 3 illustrates a detailed diagram of a first embodiment of a pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention;

Fig. 4 illustrates a detailed diagram of a second embodiment of the pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention;

Fig. 5 illustrates diagrams of an exemplary transmitted chip stream (a) at a transmitter, an exemplary error function (b), a corresponding received chip stream (c) at a receiver, a corresponding correlator output (d), a corresponding deviation of the correlator output (e), and a corresponding thresholded correlator output (f), over six bit periods;

Fig. 6 illustrates a diagram of continuously histogramming the correlator output in one embodiment of the present invention;

Fig. 7 illustrates a detailed diagram of a third embodiment of the pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention; and

Fig. 8 illustrates an alternative hardware environment for the pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention.

Fig. 9 illustrates a general diagram of a pseudo-noise encoded digital data clock recovery circuit in accordance with the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the exemplary embodiment, reference is made to the accompanying drawings which form a part hereof, and in which it is shown by way of illustration the specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized as structural changes may be made without departing from the scope of the present invention.

The present invention provides a pseudo-noise encoded digital data clock recovery circuit that recovers an original bit stream from a received chip stream. The pseudo-noise encoded digital data clock recovery circuit reliably synchronizes a bit clock, identifies a correct bit alignment, and tracks a correct bit alignment over time, for example, more than two bit periods, etc.

Exemplary embodiments and/or implementations in accordance with the principles of the present invention are set forth below. The commonality of the different embodiments and/or implementations is that the clock recovery circuit uses a bit clock generator to generate a history of correlator outputs over a plurality of bit periods. The history of the correlator outputs over the plurality of bit periods is used by a phase controller to select the most likely "correct" phase for a bit clock. The bit clock is used to sample the received signals thereby recovering/acquiring the original data from the received signals.

Fig. 1 illustrates a diagram of an exemplary communication system 100 using a pseudo-noise encoded digital data clock recovery circuit 180 in accordance with the

principles of the present invention. The communication system 100 includes a pseudo-noise encoder 120 which receives original data stream 110 (or referred to as an original bit stream). The data 110 is modulated by a pseudo-noise sequence 122 in the pseudo-noise encoder 120. In this type of modulation, '1' bits in the original bit stream are replaced by a selected pseudo-noise sequence 122, and '0' bits in the original bit stream are replaced by the complement of the selected pseudo-noise sequence 122.

The communication system 100 may include a further modulation step where an analog carrier signal is modulated by the pseudo-noise modulated data stream or sequence for effective transmission over a physical medium (e.g., PSK, FM). The data is transferred via the transmitter 130 where it is transmitted via an antenna 140 or other suitable means.

Transmitted signals 150 are received by a receive site antenna 160 or other suitable means. The signals 150 are captured by a receiver circuit 170. If there is an analog modulation step implemented in a transmitter 130, then a digital chip stream 194 is recovered from the transmitted signals 150 by a demodulation step which may be implemented in the receiver circuit 170. Then, the pseudo-noise encoded digital data clock recovery circuit 180 decodes the modulated signal (referred to as a chip stream) to obtain the original bit stream 110 via an output signal 196. In some systems, the signals 150 are first demodulated to recover the same chip stream generated by the pseudo-noise encoder 120 while in other systems, the original bit stream is recovered directly from the received analog signals in one demodulation step.

The pseudo-noise encoded digital data clock recovery circuit 180 includes a correlation circuit 182 for determining the number of matches between the predetermined pseudo-noise (PN) signal 181 and the received signal. The predetermined PN signal 181 is the same as the predetermined PN signal 122 at the transmitter end. An arithmetic circuit 184 may be used to count/accumulate the number of matches for a sample position.

In Fig. 1, the clock recovery circuit 180 also includes a decision circuit 186 which determines whether the data stream 183 should be phase-shifted within a selected window of chips to align the data stream 183 with the predetermined pseudo-noise signal 181. A reacquisition circuit 188 may be used to reacquire a preliminary bit clock signal, which includes resetting components, such as counters, and registers, etc. A location circuit 192 may be used to select an accumulator/counter aligned with a current chip position in the PN correlated chip stream. The bit clock or detection signal 196 provides output signals of the circuit 180. The output signals are used as a bit clock which has the most 'correct' phase for resampling the PN correlated chip stream to recover the original bit stream.

Fig. 2 illustrates diagrams 200 of an exemplary original bit stream 2(a) at a transmitter, a corresponding pseudo- noise sequence encoded chip stream 2(b) at a transmitter, and a corresponding correlator output 2(c), over six bit period. Diagram (a) shows an original bit stream of ones and zeros, e.g. an original bit stream of 100110. Diagram (b) shows a transmitted chip stream correlating to the ones and zeros of Diagram (a). In this type of modulation, "1" bits in the original bit stream are replaced by the true

pseudo-noise sequence, e.g. 101100111101000, and "0" bits in the original bit stream are replaced by its complement, e.g. 010011000010111. Thus, the bit rate of the modulated data stream is M times the bit rate of the original bit stream where M is the number of bits in the pseudo-noise sequence, in this example, M is fifteen (15). The recovery circuit can recover the original bit stream by looking for matches with the pseudo-noise sequence, e.g. 101100111101000, and its complement 010011000010111, within the incoming chip stream. However, if the communication channel is noisy, resulting in frequent chip errors, a more sophisticated method is needed to recover the data. Diagram (c) shows a correlator output. The correlator output indicates the degree of correlation between the received chip stream and the pseudo-noise sequence.

Fig. 3 illustrates a detailed diagram of a first embodiment of a pseudo-noise encoded digital data clock recovery circuit 300 in accordance with the principles of the present invention. In this embodiment, the pseudo-noise encoded digital data clock recovery circuit 300 correlates the received chip stream with a reference pseudo-noise sequence to generate a correlator output 307. The correlator output 307 is then compared to an upper threshold 310 and a lower threshold 315, and the resulting signals from the upper and lower thresholds are ORed together at a OR gate 320. The OR gate 320 generates a thresholded correlator output signal 321.

A modulo-15 counter 325 in a location circuit 327 is used to select an appropriate sample counter from fifteen counters 360, 361, 362, ..., 374 to increment via a decoder 330 and an associated AND gates 340, 341, 342, ..., 354. The counters 360–374 in an

arithmetic circuit 329 are incremented by logically ANDing, at the AND gates 340-354, the signal from the OR gate 320 and the signal from the decoder 330 for all sample positions within a bit period for N consecutive bit periods.

The counter, 360-374, for each sample position within a bit period is incremented when the correlator output 307 produces a spike at that sample position. A bit period counter 335 of a counter circuit 328 controls the end of the N bit periods. At that time, the values of the counters are compared with a predetermined threshold 339 by comparators 380, 381, 382, ..., 394 in the arithmetic circuit 329. The resulting signals are sent to an encoder 396, a register 397, and a comparator 398. A bit clock or detector signal 399 is generated from a decision circuit 326. Accordingly, at the end of N bit periods which is recorded by the bit period counter 335, if there is one counter, 360-374, whose value exceeds the threshold 339, when compared by the comparators 380-394, then the bit clock 399 is aligned to that counter's sample position via the encoder 396. On the other hand, if no counters, 360-374, exceed the threshold 339, then the alignment of the bit clock 399 is not adjusted. The values in the set of counters 340 through 374 taken together are henceforth referred to as a "histogram" as they represent the cumulative number of thresholded correlator output spikes over multiple bit periods as a function of sample position within the bit period. The process of creating this histogram, i.e., incrementing the counters, is henceforth referred to as "histogramming the thresholded correlator output."

In systems with multiple samples per chip (referred to as "oversampled") which will be described in details in Fig. 4, the clock recovery circuit looks for a series of consecutive samples in one bit period to see whether the corresponding counter values exceed a threshold and decide whether the phase shift of the bit clock, is needed. If a counter exceeds the threshold outside the range of counters associated with the chip position of the current bit clock, the bit clock is re-aligned at a different sample position, for example, advancing one sample position or retarding one sample position. If no counters exceed the threshold, the bit clock still remains at the same sample position.

In systems with oversampled chip streams, the correlator output histogram can be efficiently realized by implementing counters (e.g. the counters 460 through 465) for only a subset of the total sample positions of a bit period. This subset consists of a cluster of consecutive samples spanning an interval, or "window", slightly larger than one chip period. The alignment of this window, relative to the correlator output, is initially set by a reacquisition circuit (e.g. a reacquisition circuit 451 as shown in Fig. 4) based on a preliminary estimate of the most likely position of the corrector bit clock. Preferably, the alignment of this window is such that there is a margin of at least one sample position on either side of the chip period associated with the bit clock. Also, after N bit periods, the counters, such as the counters 360-374, and the registers, such as the register 397, are reset, and the histogram process starts again.

Fig. 4 illustrates a detailed diagram of a second embodiment of the pseudo-noise encoded digital data clock recovery circuit 400 in accordance with the principles of the

present invention. As shown in Fig. 4, fewer counters are used in comparison to the counters used in the embodiment shown in Fig. 3. For illustrated purposes, six counters 460-465 are used to histogram over a window of consecutive sample positions (e.g. 6 samples) which spans a subset of the total sample positions within a bit period (e.g. 60 sample positions). A window of consecutive sample positions is chosen to be larger than the bit period of one chip while a margin of one sample is at the either side of the chip period. A correlator output 407 from a correlator 405 in a correlation circuit 402 is compared to an upper threshold 410 and a lower threshold 415. The resulting signals are ORed together at a OR gate 420.

A modulo-60 counter 425 in a location circuit 424 is used to select an appropriate sample counter from the six counters 460-465 to increment via a decoder 430 and an associated AND gates 440-445 in an arithmetic circuit 447. The counters 460-465 in the arithmetic circuit 447 are incremented by logically ANDing, at the AND gates 440-445, the signal from the OR gate 420 and the signal from the decoder 430 for all sample positions within a bit period for N consecutive bit periods. The counter, 460-445, for each sample position within a bit period is incremented when the correlator output 407 produces a spike at that sample position.

As shown in Fig. 4, a system may employ four samples per chip and implement a six-sample histogram window. In such a system, one would expect to see spikes at the correlator output 407 most often during the four consecutive sample positions when the bit period of the incoming chip stream 401 is aligned with the reference pseudo-noise

sequence 406 in the correlator 405. During the initial acquisition of the bit clock from the received chip stream 401, the histogram window can be initially placed so as to bracket the four sample positions where 'true' correlator output spikes are expected. The correlator output spikes represent the alignment of the bit period in the received chip stream 401 with the reference pseudo-noise sequence 406. This initial placement of the window may be based on some quick means of guessing where the true correlator output spikes are expected. Using this example, one way of initially placing the window would be to center the window around the first three or four consecutive correlator output spikes observed at the correlator output 407. After this initial placement, the correlator output 407 is histogrammed for N bit periods for those sample positions that fall within the window.

Accordingly, at the end of the N bit periods which is controlled by a bit period counter 435 in a counter circuit 434, a bit clock 499 is centered within the sample positions whose histogram counters 460–465 exceed a threshold 449 as depicted in the arithmetic circuit 447. If the alignment of the resulting bit clock is not centered within the window, then the window is shifted via sending an adjust-forward signal, ADJ_FWD 490, or an adjust-backward signal, ADJ_BCK 492, from a decision circuit 448 to the counter 425. Two AND gates 494, 496 are used to make sure that the window shift occurs at the end of the histogram pass. The counter 425 outputs a signal which adjusts the sample histogram window. This window shift requires a means of determining whether the initial or the prior window placement is incorrect, and that the acquisition

step should be repeated. One of the means of doing so is to declare the initial window placement invalid if a certain number of consecutive histogram passes (each spanning N bit periods) are performed but the histogram counters 460–465 do not exceed the required threshold. At this point, a set/reset device 498 in the reacquisition circuit 451 is used. The inverted signals from the comparators 480-485 are sent to an AND gate 450 along with the proper sequence of signals through additional reacquisition devices 452, 454, 456, 458 in the reacquisition circuit 451. It is appreciated that other means of placing and shifting the window can be used within the scope of the present invention.

Fig. 5 illustrates diagrams of an exemplary transmitted chip stream (a) at a transmitter, an exemplary error function (b), and a corresponding received chip stream (c) at a receiver, over six bit periods. As shown, the transmitted chip stream (a) is different from the received chip stream (c) because the communication channel or transmission media is noisy resulting in frequent chip errors (e.g. the chip error rate is 0.2). An exemplary error function ChpErr (b) indicates where chips in the received chip stream are inverted due to the noise. The greater the chip error rate, the more difficult it is to recognize the pseudo-noise sequence or its complement in the received chip stream (rxChip) (c).

The corresponding correlator output (d) can then be sent to the arithmetic circuit of the clock recovery circuit as described above. In one embodiment as previously described, counters are used to count the number of thresholded correlator output spikes. In another embodiment, the correlator output can be histogrammed directly by using

accumulators to integrate the correlator output directly in each sample position over multiple bit periods, instead of counters which increment in response to a spike at he thresholded correlator output. This may need more register bits to implement, but the result maintains a more accurate history of the correlator output. At each sample position (within the histogram window if using a subset of sampling positions in a bit period), a deviation value ΔCOR is added to the corresponding accumulator which represents the degree of correlation between the received chip stream and the pseudo-noise sequence or its complement. More specifically, ΔCOR is a measure of the deviation of the correlator output, COR, from the center of its range. For example, in a system with fifteen (15) chips per bit period, the correlator produces a value for COR that ranges from 0 to 15, reflecting the number of chips in the correlator's shift register that match the chips of the pseudo-noise sequence as shown in Diagram (d). In the system of using accumulators, the ΔCOR is the absolute value of 7.5 (1/2 of 15) minus COR rounded down to the nearest whole number as shown in Diagram (e). Diagram (f) shows a binary signal that results from applying the upper and lower thresholds to COR. This signal, i.e. the thresholded correlator output, controls the incrementing of the histogram counters in the embodiments using counters.

Fig. 6 illustrates an implementation of one of the histogram accumulators described above which integrates the correlator output continuously instead of over a finite number of bit periods. In order to do this without overflowing histogram accumulators 620, at each pass through a histogram window, the current pass of

correlator outputs 610 are added to the histogram at an adder 640. Therefore, the previous correlator outputs, which are already a part of the histogram, are weighted 650 by a fractional value 630 whereby the fraction decreases geometrically in each subsequent bit period. An example of implementing this is to multiply each counter/accumulator 620 by a fixed fraction 630 in a bit period before the correlator outputs pass through the histogram window. It is appreciated that a person skilled in the art of digital signal processing would know that this is equivalent to applying a first-order low pass filter (LPF) to the correlator output. For example, if the fraction used is seven-eighths (7/8), then a preferred implementation is to subtract from each histogram accumulator a right shifted version of itself, i.e. a right shifted by 3, before adding the next correlator output.

It is appreciated that other suitable implementations for histogramming accumulators can be used without departing from the scope of the present invention. For example, in another implementation, it is sufficient to right shift the histogram accumulators one bit, i.e. multiplying by ½, once every few bit periods. In this case, the threshold against which the histogram accumulators are compared would have to be adjusted depending on the number of bit periods since the last right shift.

Fig. 7 illustrates a detailed diagram of a third embodiment of the pseudo-noise encoded digital data clock recovery circuit 700 in accordance with the principles of the present invention. The example shown implements four (4) samples per chip and a histogram window size of seven (7) samples. In systems with multiple samples per chip,

the phase of a bit clock can be more accurately tracked by calculating the average sample position after each pass through a histogram window. The average sample position is the sum of the histogram accumulator values weighted by their associated sample positions divided by the sum of the histogram accumulator values weighted by one.

To implement this in a system with fifteen (15) chips per bit, the correlator produces a value COR that ranges from 0 to 15, reflecting the number of chips in the correlator's shift register that match the chips with the pseudo-noise sequence.

As shown in Fig. 7, a ΔCOR 710 in a correlation circuit 703 is the absolute value 708 of 7.5 (1/2 of 15) 704 minus a COR 702 rounded down to the nearest whole number 706. The ΔCOR 710 then passes through the seven low pass filter (LPF) counter/accumulator 720–732 as shown in Fig. 6.

Each sample position within a histogram window is assigned a number which denotes its position in the window. For example, in a histogram window of seven sample positions 740–752 as shown, the successive sample positions can be numbered as -3, -2, -1, 0, 1, 2, and 3. At the end of each pass through the histogram window, two sums are calculated in a arithmetic circuit 719. The first sum 762 is the value 740 from the first histogram accumulator 720 times -3, plus the value 742 in the second histogram accumulator 722 times -2, plus the value 744 from the third histogram accumulator 724 times -1, plus the value 746 from the fourth histogram accumulator 726 times 0, plus the value 748 from the fifth histogram accumulator 728 times 1, plus the value 750 from the

sixth histogram accumulator 730 times 2, and plus the value 752 from the seventh histogram accumulator 732 times 3.

The second sum 760 is the sum of the values from all seven accumulators 720-732. The average or optimal sample position where the correlator output is used to recover the original bit stream is indicated by the result of dividing the first sum 762 by the second sum 760. If the result is between -0.5 and +0.5, then the phase of a bit clock 799 remains the same, for example, at the center of the histogram window. If the result is between 0.5 and 1.5, then the phase of the bit clock and the histogram window is retarded by one sample position by asserting a signal ADJ_CLK from a decision circuit 777 to a counter 788 in a location circuit 714. If the result is between -1.5 and -0.5, then the phase of the bit clock is advanced by one sample position by asserting a signal ADJ_FWD as well as a signal ADJ_CLK from the decision circuit 777 to the counter 788 in the location circuit 714.

A decoder 715 in the location circuit 714 is used to enable the integration of the correlator output at each sample position. The decoder 715 is controlled by the output of the counter 788. If the accumulators 720 through 732 fail to register sufficient counts to indicate alignment of the correct bit clock with the histogram window, a reacquisition can be performed by a reacquisition circuit 791 by reacquisition circuitry components 790–798, similar to the reacquisition circuit components 452-458 shown in Fig. 4.

It is appreciated that the technique of aligning a bit clock over a plurality of bit periods can be varied within the scope of the present invention. For example, it may not

maintain a set of histogram accumulators for a histogram window. A result for the correct sample position can be produced by maintaining registers for the position weighted and non-weighted sums and updating the two registers with each pass through the histogram window. At each sample position within the window, the correlator output is added directly to the non-weighted sum and multiplied by its sample position before adding to the weighted sum. These two sums can be maintained continuously by multiplying by a fraction before each pass in the same fashion as histogram accumulators as described above.

Fig. 8 illustrates an alternative hardware environment 800 for a pseudo-noise encoded digital data clock recovery circuit 830 in accordance with the principles of the present invention. Such hardware environment may include a processor 810, a data storage device 820, a memory (RAM) 840, and an input device 850. The clock recovery circuit 830 may operate under the control of an operating system which executes one or more computer programs. The operating system and the computer programs may be tangibly embodied in a computer-readable medium or carrier, e.g. one or more of the fixed or removable data storage devices 820, or other suitable data storage or data communication devices. Both operating system and the computer programs may be loaded from the data storage devices 820 into the memory 840 for execution by the processor 810. Those skilled in the art would recognize that the memory 840 is optional or may be a memory device embedded or otherwise coupled to the pseudo-noise encoded digital data recovery circuit 830. Further, both the operating system and the computer

programs may comprise instructions which, when read and executed by the processor 810, cause the clock recovery circuit 830 to perform the steps necessary to execute the steps or circuit components of the present invention. An input signal 801 is input into the clock recovery circuit 830, and an output signal 860 is output from the clock recovery circuit 830.

Although an exemplary system configuration is illustrated in Fig. 8, those skilled in the art would recognize that any number of different system configurations performing similar functions may be used in accordance with the present invention.

Fig. 9 illustrates a general diagram of a pseudo-noise encoded digital data clock recovery circuit 900 in accordance with the principles of the present invention. The recovery circuit 900 includes a correlator 902 for correlating a pseudo-noise sequence 904, which modulates an original bit stream, with a received chip stream 906. A bit clock phase controller 912 is coupled to the correlator 902. a bit clock generator 908 receives the output of the bit clock phase controller 912 and generates a bit clock 910 which determines a sampling position of the received chip stream 906 to recover the original bit stream from the received chip stream 906. The bit clock phase controller 912 is coupled to the output of the bit clock generator 908 and feeds a control signal back to the bit clock generator 908. The bit clock phase controller 912 maintains alignment between the received chip stream 906 and the pseudo-noise sequence 904 over a plurality of bit periods of the received chip stream 906 by adjusting the sample position of the bit clock 910.

The correlator 902 may include the correlation circuit as described above in Figs. 1, 3, 4, and 7. Also, the bit clock phase controller 912 may include the arithmetic circuit, the decision circuit, and the counter circuit as described above. Further, the bit clock generator 908 may include the location circuit as described above. It is appreciated that the layout of the circuits can be varied within the scope of the invention.

The foregoing description of the exemplary embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not with this detailed description, but rather by the claims appended hereto.

Claims

What is claimed is:

1. A method for recovering an original bit stream from a received chip stream in a communication system, comprising the steps of:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

2. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming a correlator output over all possible sample positions for the bit clock.

3. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming a correlator output over a finite window of sample positions for the bit clock.

4. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

5. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

6. The method of claim 1, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

7. The method of claim 1, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

8. The method of claim 6, wherein the step of synchronizing the bit clock is based on the histogram of the counters that exceed a preset threshold.

9. The method of claim 7, wherein the step of synchronizing the bit clock is based on the histogram of the accumulators that exceed a preset threshold.

10. The method of claim 1, wherein the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

11. The method of claim 2, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

12. The method of claim 2, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

13. The method of claim 3, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

14. The method of claim 3, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

15. The method of claim 6, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

16. The method of claim 6, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

17. The method of claim 7, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

18. The method of claim 7, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

19. The method of claim 8, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

20. The method of claim 8, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

21. The method of claim 9, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

22. The method of claim 9, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

23. The method of claim 10, wherein the step of maintaining the history of correlation includes histogramming a correlator output for a finite number of bit periods and restarting histogramming after the finite number of bit periods.

24. The method of claim 10, wherein the step of maintaining the history of correlation includes histogramming continuously by digitally low pass filtering a correlator output.

25. The method of claim 2, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

26. The method of claim 2, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

27. The method of claim 3, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

28. The method of claim 3, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

29. The method of claim 8, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

30. The method of claim 8, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

31. The method of claim 9, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

32. The method of claim 9, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

33. The method of claim 10, further comprising the step of providing a threshold, comparing the correlator output to the threshold, and generating a thresholded correlator

output, wherein the step of maintaining the history of correlation includes histogramming the thresholded correlator output with a corresponding counter.

34. The method of claim 10, wherein the step of maintaining the history of correlation includes histogramming the correlator output directly with a plurality of accumulators.

35. The method of claim 2, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of counters that exceed a preset threshold.

36. The method of claim 2, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of accumulators that exceed a preset threshold.

37. The method of claim 2, wherein the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

38. The method of claim 3, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of counters that exceed a preset threshold.

39. The method of claim 3, wherein the step of synchronizing the bit clock is based on the histogram of a plurality of accumulators that exceed a preset threshold.

40. The method of claim 3, wherein the step of synchronizing the bit clock is based on a calculated average sample position for the bit clock.

41. A pseudo-noise encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream, comprising:

a correlator for correlating a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence modulating the original bit stream;

a phase controller, coupled to the correlator, being configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods; and

a bit clock generator, coupled to the phase controller, for generating a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator using the histogram of the correlator output to select/adjust the sample position for the bit clock.

42. The circuit of claim 41, wherein the phase controller includes a plurality of counters to histogram the correlator output over all sample positions in a bit period for the plurality of consecutive bit periods, each of the counters corresponding to each of the sample positions within the bit period.

43. The circuit of claim 42, wherein each of the counters is incremented when a

corresponding thresholded correlator output generates a spike at the corresponding sample position.

44. The circuit of claim 43, wherein the bit clock generator adjusts the sample position of the bit clock to a position where the corresponding counter exceeds a threshold.

45. The circuit of claim 44, wherein the bit clock generator retains the same sample position of the bit clock where no counters exceed the threshold.

46. The circuit of claim 41, wherein the phase controller includes a plurality of counters to histogram the correlator output over a finite window of sample positions for the bit clock.

47. The circuit of claim 41, wherein the phase controller histograms the correlator output for a finite number of bit periods and restarts histogramming after the finite number of bit periods.

48. The circuit of claim 41, wherein the phase controller histograms continuously by digitally low pass filtering the correlator output.

49. The circuit of claim 41, further comprising a comparator which compares the correlator output to a threshold and generates a thresholded correlator output, wherein the phase controller histograms the thresholded correlator output with a plurality of counters.

50. The circuit of claim 41, wherein the phase controller includes a plurality of accumulators to histogram the correlator output directly.

51. The circuit of claim 49, wherein the bit clock is based on the histogram of the counters that exceed a preset threshold.

52. The circuit of claim 50, wherein the bit clock is based on the histogram of the accumulators that exceed a preset threshold.

53. The circuit of claim 41, wherein the bit clock is based on a calculated average sample position for the bit clock.

54. A communication system, comprising:

a transmitter, the transmitter modulating an original bit stream into a transmitted chip stream by a pseudo-noise sequence, the transmitted chip stream being transmitted to a receiver via a transmission media;

the transmission media;

the receiver receiving a received chip stream; and

a clock recovery circuit being coupled to the receiver, the clock recovery circuit recovering the original bit stream from the received chip stream, comprising:

a correlator for correlating a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence modulating the original bit stream;

a phase controller, coupled to the correlator, being configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods; and

a bit clock generator, coupled to the phase controller, for generating a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator using the histogram of the correlator output to select/adjust the sample position for the bit clock.

55. A computer program storage medium readable by a computing system and encoding a computer program of instructions for executing a computer process for recovering an original bit stream from a received chip stream, the computer process comprising:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

56. A computer data signal embodied in a carrier wave readable by a computing system and encoding a computer program of instructions for executing a computer process for recovering an original bit stream from a received chip stream, the computer process comprising:

maintaining a history of correlation of the received digital chip stream with a pseudo-noise sequence over more than two bit periods; and

synchronizing a bit clock by using the history of correlation.

ABSTRACT

A pseudo-noise (PN) encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream includes a correlator, a phase controller, and a bit clock generator. The correlator correlates a pseudo-noise sequence with the received chip stream and generating a correlator output. The pseudo-noise sequence modulates the original bit stream. The phase controller is configured and arranged to histogram the correlator output of the correlator over the plurality of bit periods. The bit clock generator generates a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream. The bit clock generator uses the histogram of the correlator output to select/adjust the sample position for the bit clock. Accordingly, the pseudo-noise encoded digital data clock recovery circuit reliably synchronizes the bit clock, identifies a correct bit alignment, and tracks a correct bit alignment over time, for example, more than two bit periods, etc.

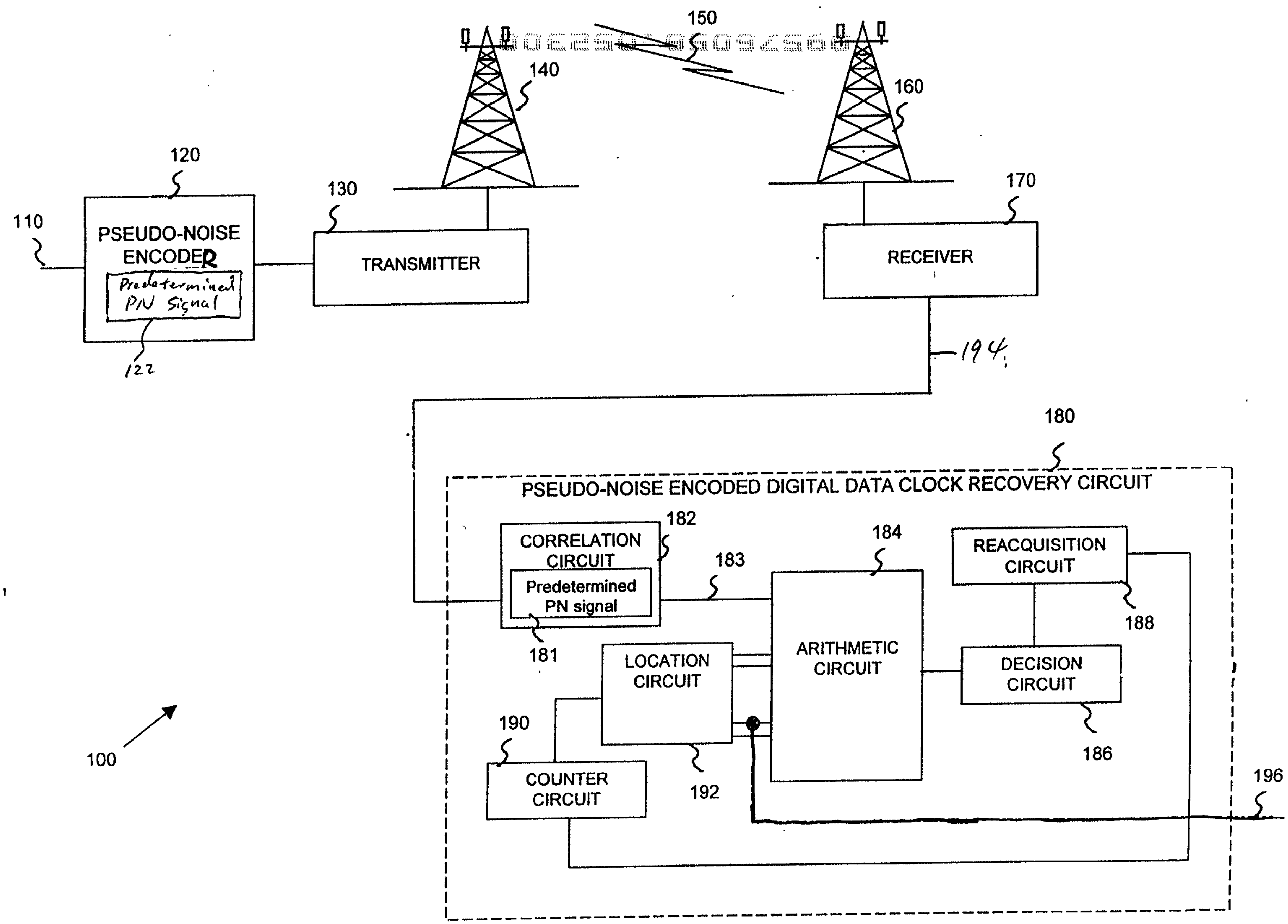

110
120
PSEUDO-NOISE ENCODER
Predetermined PN Signal
122
130
TRANSMITTER
140
150
160
170
RECEIVER
194
180
PSEUDO-NOISE ENCODED DIGITAL DATA CLOCK RECOVERY CIRCUIT
182
CORRELATION CIRCUIT
Predetermined PN signal
181
183
184
ARITHMETIC CIRCUIT
REACQUISITION CIRCUIT
188
DECISION CIRCUIT
186
LOCATION CIRCUIT
192
190
COUNTER CIRCUIT
196
100

Fig. 1

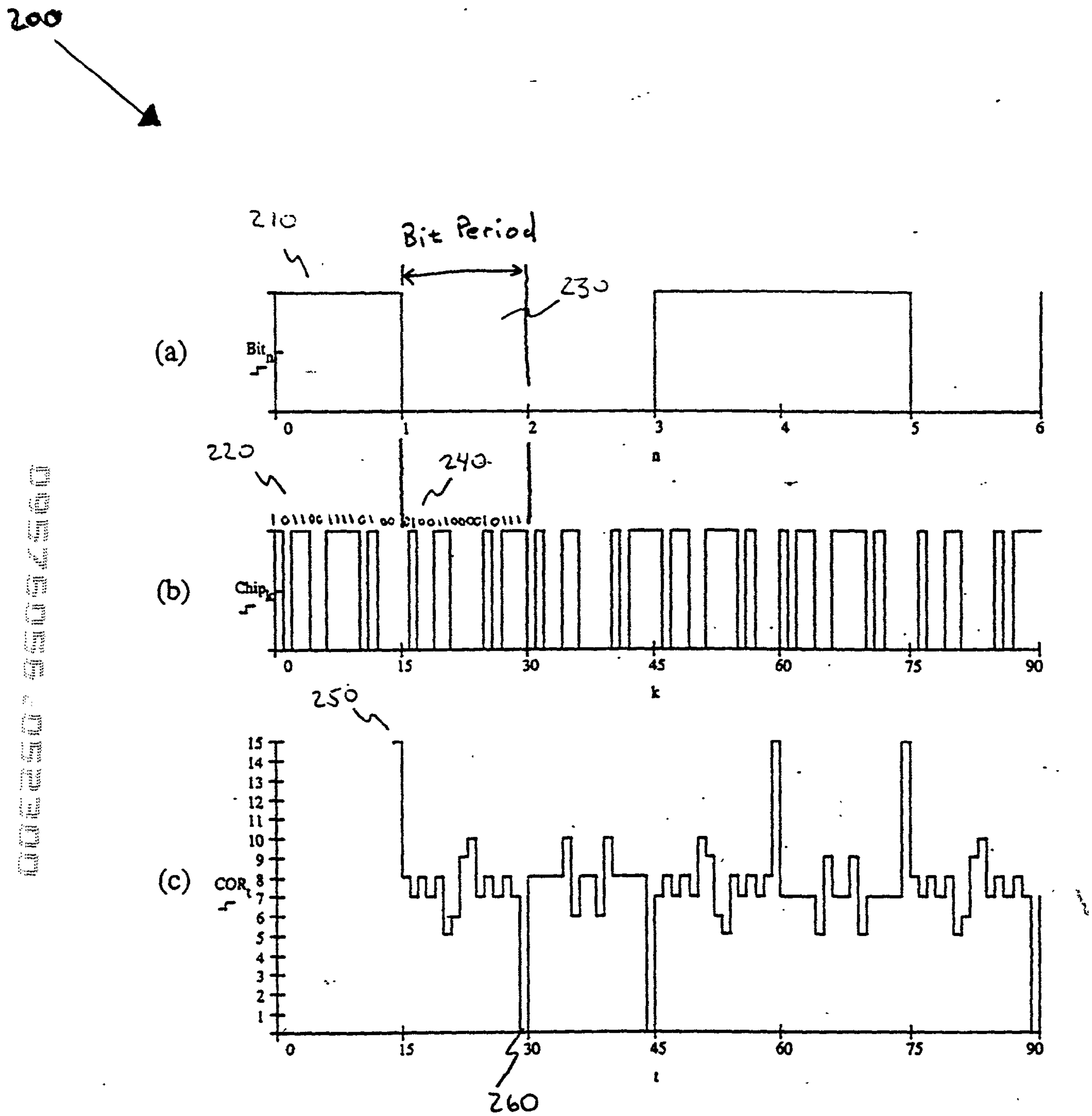


Fig. 2

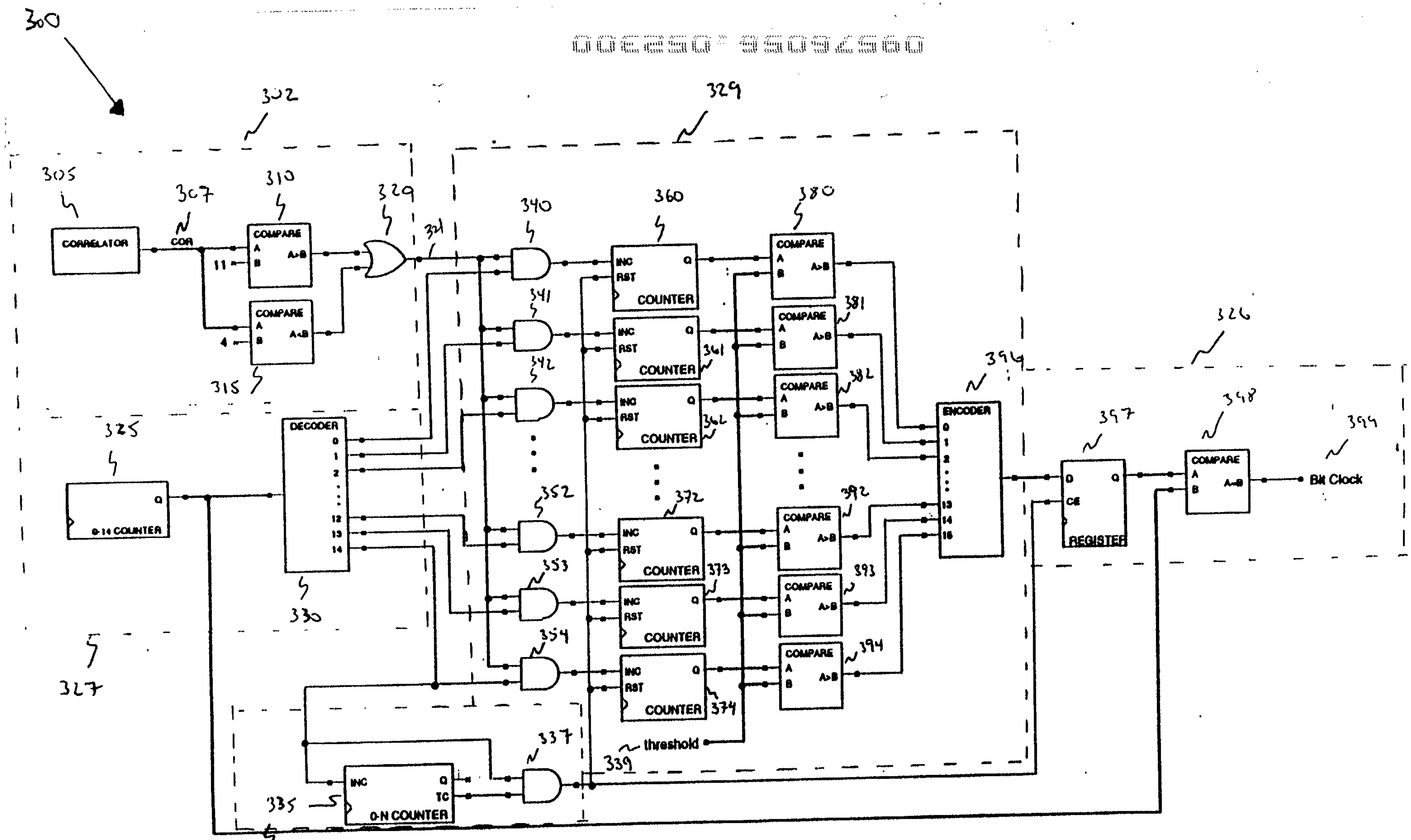

300
302
329
305
CORRELATOR
307
COR
310
COMPARE
A
B
A>B
11
COMPARE
A
B
A<B
4
315
329
321
325
0-14 COUNTER
Q
DECODER
0
1
2
12
13
14
330
327
340
341
342
352
353
354
360
INC
RST
COUNTER
Q
361
362
372
373
374
380
381
382
392
393
394
threshold
339
337
335
INC
Q
TC
0-N COUNTER
328
396
ENCODER
0
1
2
13
14
15
326
397
D
Q
CE
REGISTER
398
COMPARE
A>B
399
Bit Clock

Fig. 3

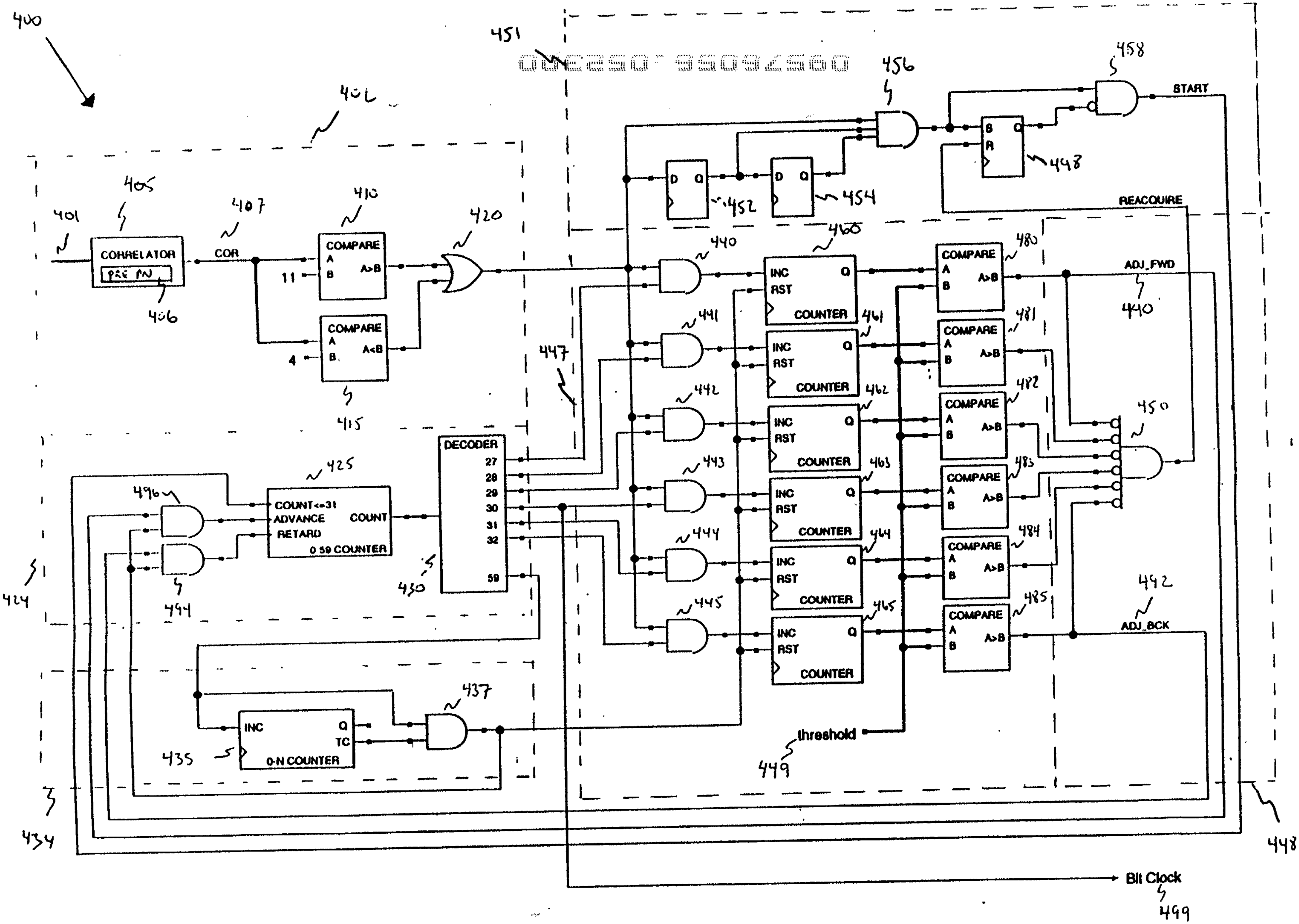
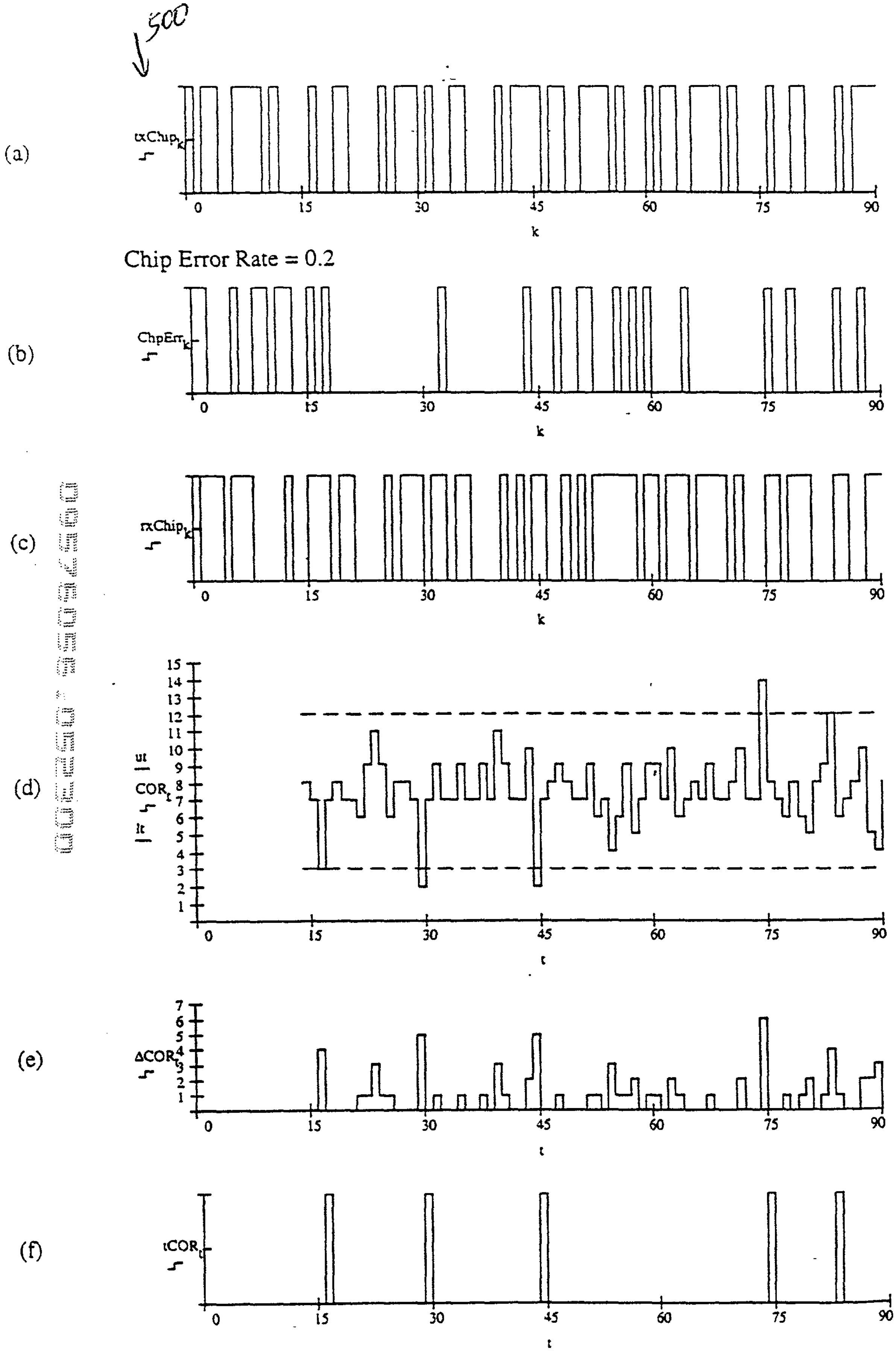

CORRELATOR
PRE PN
COR
COMPARE
A
B
A>B
A<B
11
4
DECODER
27
28
29
30
31
32
59
COUNT<=31
ADVANCE
RETARD
COUNT
0 59 COUNTER
INC
Q
TC
0-N COUNTER
RST
COUNTER
D
S
R
START
REACQUIRE
ADJ_FWD
ADJ_BCK
threshold
Bit Clock

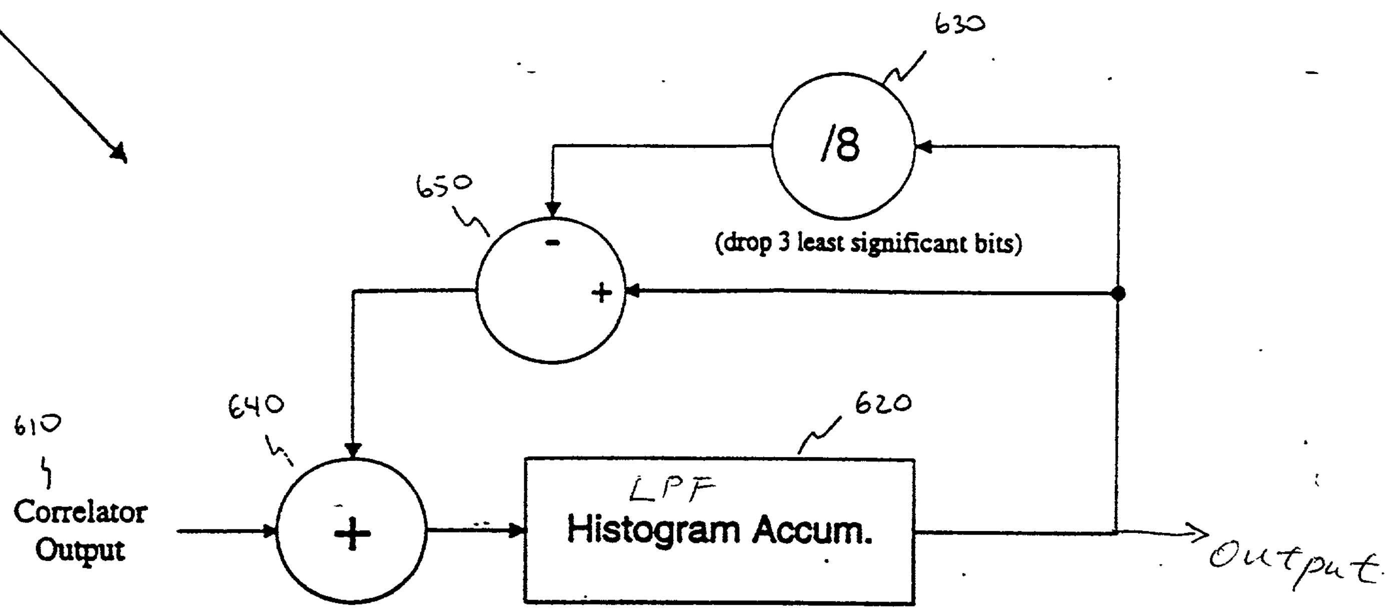
Fig. 4



500
(a)
txChip_k
0 15 30 45 60 75 90
k
Chip Error Rate = 0.2
(b)
ChpErr_k
0 15 30 45 60 75 90
k
(c)
rxChip_k
0 15 30 45 60 75 90
k
(d)
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
ut
COR_t
lt
0 15 30 45 60 75 90
t
(e)
7 6 5 4 3 2 1
ΔCOR_t
0 15 30 45 60 75 90
t
(f)
tCOR_t
0 15 30 45 60 75 90
t

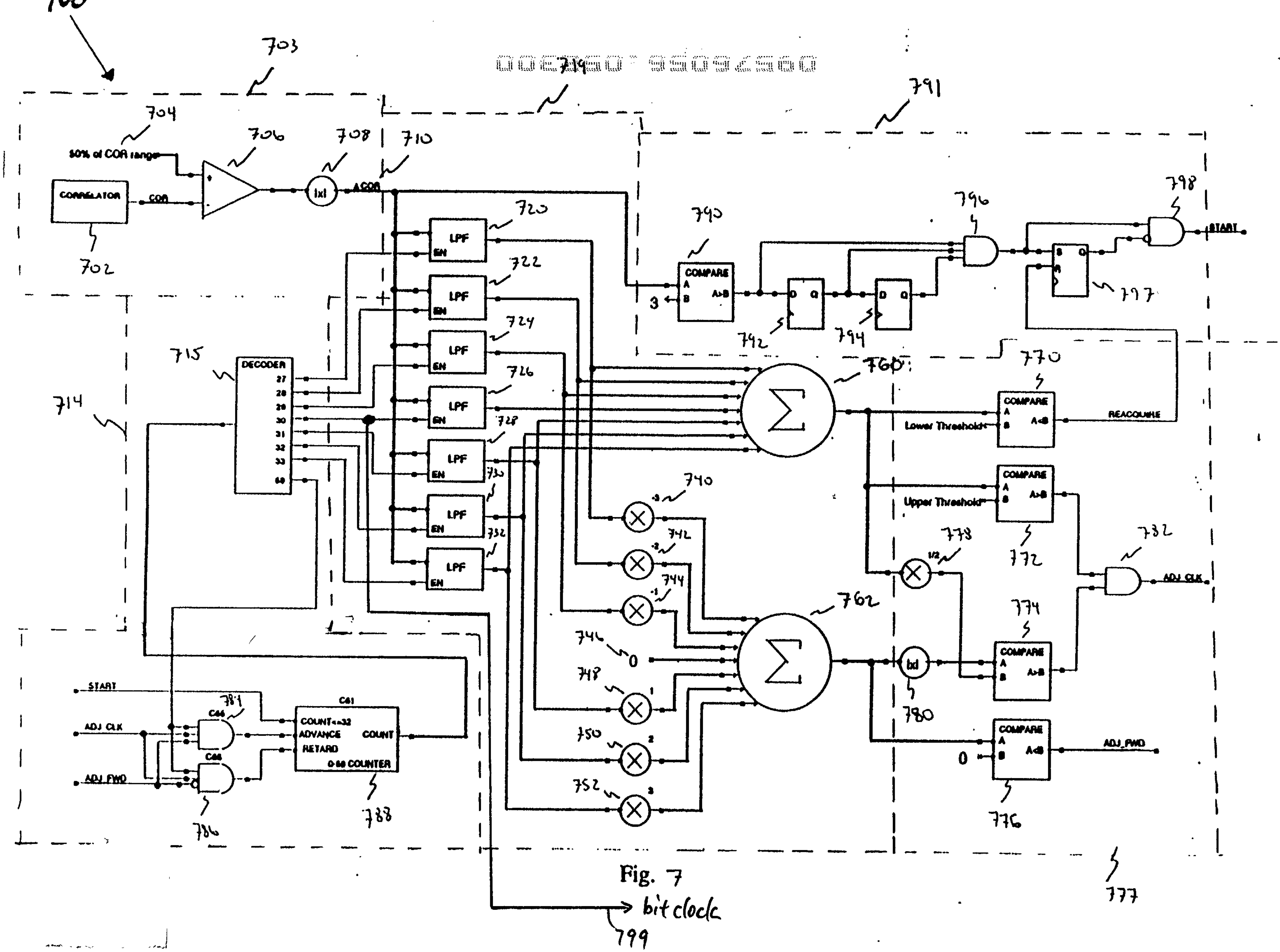
Fig. 5

600



630
/8
(drop 3 least significant bits)
650
-
+
640
620
610
Correlator Output
+
LPF
Histogram Accum.
Output

Fig. 6



700
703
704
50% of COR range
CORRELATOR
COR
702
706
708
|x|
710
ACOR
714
715
DECODER
27
28
29
30
31
32
33
60
LPF
EN
720
722
724
726
728
730
732
790
COMPARE
A
B
A>B
3
792
794
D
Q
796
797
S
R
798
START
791
760
762
770
772
774
776
Lower Threshold
Upper Threshold
A<B
REACQUIRE
778
1/2
780
732
ADJ CLK
ADJ_FWD
0
740
742
744
746
748
750
752
-3
-2
-1
1
2
3
784
786
C44
C45
C61
COUNT<=32
ADVANCE
RETARD
COUNT
0-60 COUNTER
788
777
bit clock
799

Fig. 7

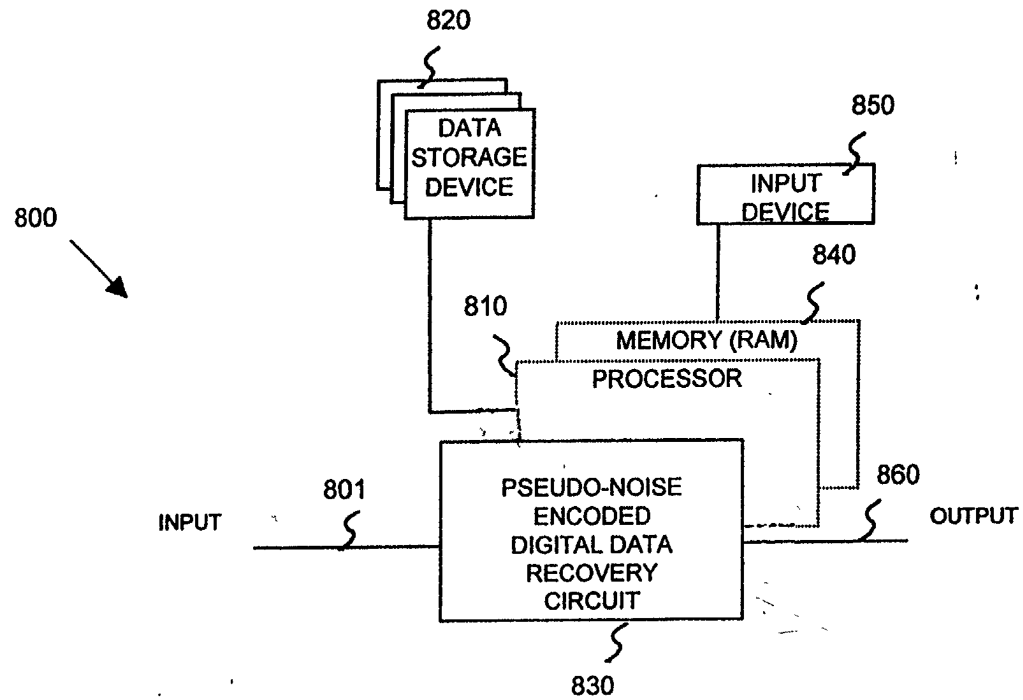

800
820
DATA
STORAGE
DEVICE
850
INPUT
DEVICE
840
810
MEMORY (RAM)
PROCESSOR
801
INPUT
PSEUDO-NOISE
ENCODED
DIGITAL DATA
RECOVERY
CIRCUIT
860
OUTPUT
830

Fig. 8

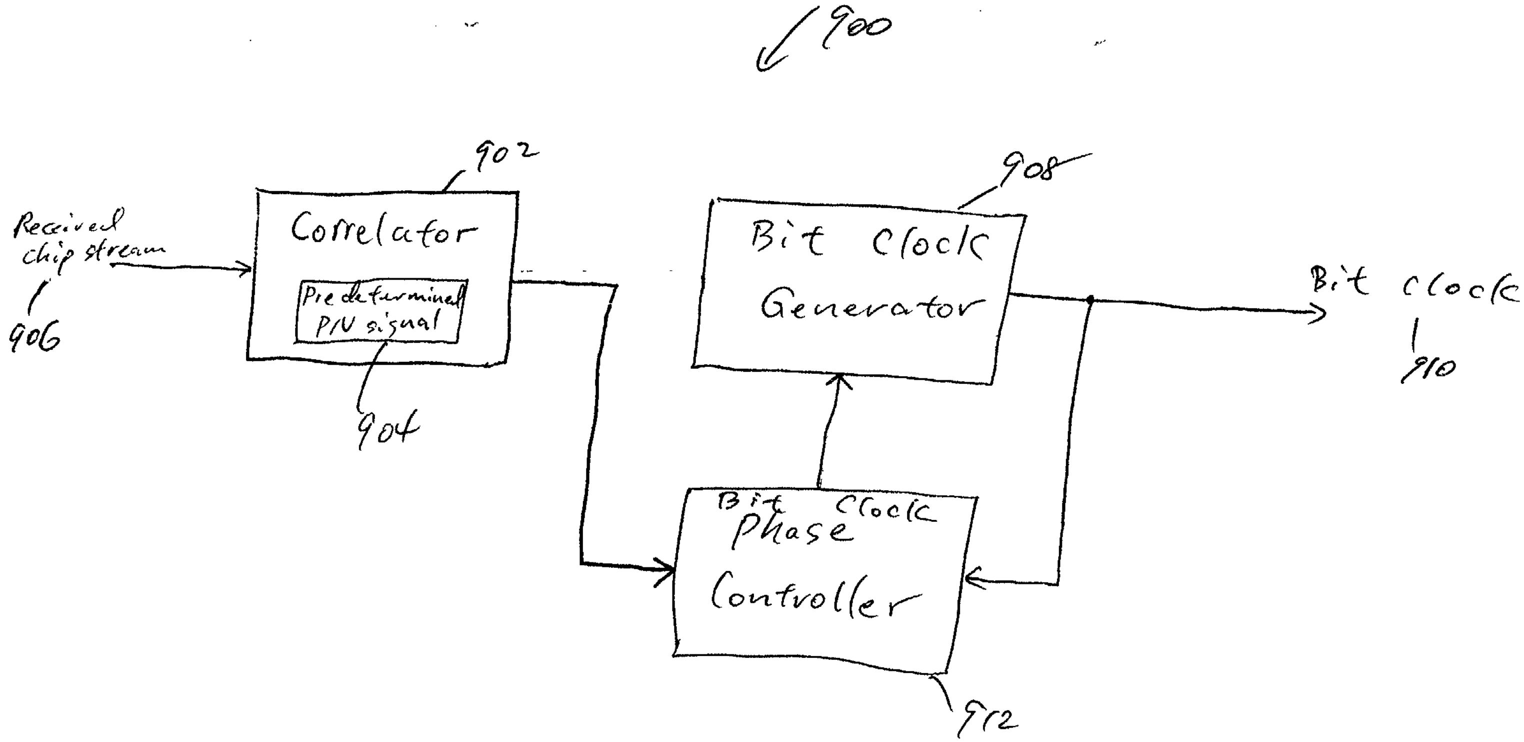

900
902
Correlator
Predetermined P/N signal
904
Received chip stream
906
908
Bit Clock Generator
Bit clock
910
Bit Clock Phase Controller
912

FIG. 9

Attorney Docket No. 30019.100USU1

MERCHANT & GOULD P.C.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **PSEUDO–NOISE ENCODED DIGITAL DATA CLOCK RECOVERY**

The specification of which

a. ☐ is attached hereto

b. ☒ is entitled **PSEUDO–NOISE ENCODED DIGITAL DATA CLOCK RECOVERY**, having an attorney docket number **30019.100USU1**.

c. ☐ was filed on as application serial no. and was amended on (if applicable) (in the case of a PCT–filed application) described and claimed in international no. filed and as amended on (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above–identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications have been filed.

b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	DATE OF ISSUE (day, month, year)

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	DATE OF FILING (Day, Month, Year)
60/135,571	24 May 1999

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Albrecht, John W.	Reg. No. 40,481	Lacy, Paul E.	Reg. No. 38,946
Anderson, Gregg I.	Reg. No. 28,828	Larson, James A.	Reg. No. 40,443
Ansems, Gregory M.	Reg. No. 42,264	Liepa, Mara E.	Reg. No. 40,066
Batzli, Brian H.	Reg. No. 32,960	Lindquist, Timothy A.	Reg. No. 40,701
Beard, John L.	Reg. No. 27,612	Lycke, Lawrence E.	Reg. No. 38,540
Berns, John M.	Reg. No. 43,496	McAuley, Steven A.	Reg. No. P-46,084
Black, Bruce E.	Reg. No. 41,622	McDonald, Daniel W.	Reg. No. 32,044
Branch, John W.	Reg. No. 41,633	McIntyre, Jr., William F.	Reg. No. P-44,921
Bremer, Dennis C.	Reg. No. 40,528	Mueller, Douglas P.	Reg. No. 30,300
Bruess, Steven C.	Reg. No. 34,130	Pauly, Daniel M.	Reg. No. 40,123
Byrne, Linda M.	Reg. No. 32,404	Pendergast, Paul	Reg. No. 46,068
Carlson, Alan G.	Reg. No. 25,959	Phillips, John B.	Reg. No. 37,206
Caspers, Philip P.	Reg. No. 33,227	Plunkett, Theodore	Reg. No. 37,209
Chiapetta, James R.	Reg. No. 39,634	Pytel, Melissa J.	Reg. No. 41,512
Clifford, John A.	Reg. No. 30,247	Qualey, Terry	Reg. No. 25,148
Cochran, William W.	Reg. No. 26,652	Reich, John C.	Reg. No. 37,703
Daignault, Ronald A.	Reg. No. 25,968	Reiland, Earl D.	Reg. No. 25,767
Daley, Dennis R.	Reg. No. 34,994	Schmaltz, David G.	Reg. No. 39,828
Dalglish, Leslie E.	Reg. No. 40,579	Schuman, Mark D.	Reg. No. 31,197
Daulton, Julie R.	Reg. No. 36,414	Schumann, Michael D.	Reg. No. 30,422
DeVries Smith, Katherine M.	Reg. No. 42,157	Scull, Timothy B.	Reg. No. 42,137
DiPietro, Mark J.	Reg. No. 28,707	Sebald, Gregory A.	Reg. No. 33,280
Edell, Robert T.	Reg. No. 20,187	Skoog, Mark T.	Reg. No. 40,178
Epp Ryan, Sandra	Reg. No. 39,667	Spellman, Steven J.	Reg. No. 45,124
Glance, Robert J.	Reg. No. 40,620	Stoll-DeBell, Kirstin L.	Reg. No. 43,164
Goggin, Matthew J.	Reg. No. 44,125	Storer, Shelley D.	Reg. No. 45,135
Golla, Charles E.	Reg. No. 26,896	Sumner, John P.	Reg. No. 29,114
Gorman, Alan G.	Reg. No. 38,472	Sumners, John S.	Reg. No. 24,216
Gould, John D.	Reg. No. 18,223	Swenson, Erik G.	Reg. No. 45,147
Gregson, Richard	Reg. No. 41,804	Tellekson, David K.	Reg. No. 32,314
Gresens, John J.	Reg. No. 33,112	Trembath, Jon R.	Reg. No. 38,344
Hamre, Curtis B.	Reg. No. 29,165	Underhill, Albert L.	Reg. No. 27,403
Hillson, Randall A.	Reg. No. 31,838	Vandenburgh, J. Derek	Reg. No. 32,179
Holzer, Jr., Richard J.	Reg. No. 42,668	Wahl, John R.	Reg. No. 33,044
Johnston, Scott W.	Reg. No. 39,721	Weaver, Karrie G.	Reg. No. 43,245
Kadievitch, Natalie D.	Reg. No. 34,196	Welter, Paul A.	Reg. No. 20,890
Karjeker, Shaukat	Reg. No. 34,049	Whipps, Brian	Reg. No. 43,261
Kastelic, Joseph M.	Reg. No. 37,160	Wickhem, J. Scot	Reg. No. 41,376
Kettelberger, Denise	Reg. No. 33,924	Williams, Douglas J.	Reg. No. 27,054
Keys, Jeramie J.	Reg. No. 42,724	Witt, Jonelle	Reg. No. 41,980
Knearl, Homer L.	Reg. No. 21,197	Wu, Tong	Reg. No. 43,361
Kowalchyk, Alan W.	Reg. No. 31,535	Xu, Min S.	Reg. No. 39,536
Kowalchyk, Katherine M.	Reg. No. 36,848	Zeuli, Anthony R.	Reg. No. 45,255

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Merchant & Gould P.C. to the contrary.

Please direct all correspondence in this case to Merchant & Gould P.C. at the address indicated below:

Min S. Xu, Esq.
Merchant & Gould P.C.
P. O. Box 2903
Minneapolis, MN 55402 0903

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2	Full Name Of Inventor	Family Name BALLINGER	First Given Name David	Second Given Name Gordon
0	Residence & Citizenship	City San Francisco	State or Foreign Country California	Country of Citizenship U.S.A.
1	Post Office Address	Post Office Address 702B Broderick Street	City San Francisco	State & Zip Code/Country CA/94117/USA

Signature of Inventor 201: D. Gordon Ballinger

Date: May 23, 2000

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden of proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.